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Appl. No. 10/711,618 Amdt. dated May 9, 2006 Reply to Office action of January 25, 2006

Amendments to the Specification:

In paragraph [19]:

The loading module 36 comprises a loading capacitor CL and two loading resistors RL1 and RL2 used as a voltage divider. The loading capacitor CL is connected between the output node NOUT and the second voltage source VSS. Typically, the second voltage source VSS provides a ground voltage or a low voltage level. The first loading resistor RL1 is coupled between the output node NOUT and the node NF1. The second loading resistor RL2 is coupled between the feedback node NF1 and the second voltage source VSS. These two loading resistors RL1 and RL2 act as a voltage divider, hence the voltage on the feedback node NF1 is a value between the output voltage and the voltage provided by the second voltage source VSS. The voltage divided by the first and the second loading resistors RL1, RL2 is then fed back to the amplifier circuit 32. Please refer to Fig.2 again. The source of the first discharge transistor 41 and the drain of the second discharge transistor 42 are connected to each other on the feedback node NF1 wherein the first discharge transistor 41 and the second discharge transistor 42 are both NMOS-NOMS transistors. The gate of the first discharge transistor 41 is electrically connected to the inverter 40, and the drain is electrically connected to the output node NOUT. The gate of the second discharge transistor 42 is also electrically connected to the inverter 40, and the source is electrically connected to the second voltage source VSS. The inverter 40 is used to transform the enable signal ENABLE into an inverse enable signal IN_ENABLE and to output the inverse enable signal IN_ENABLE to the first discharge transistor 41 and the second discharge transistor 42. Therefore, the voltage level of the inverse enable signal IN_ENABLE generated by the inverter 40 decides whether the first discharge transistor 41 and the second discharge transistor 42 are turned on or not.